

**REMARKS**

The present invention discloses contact interconnect structures that achieve reliable electrical contacts including two active contact regions in CMOS integrated circuits. The present invention novel structure further allows improved patterning, etching and metal filling characteristics.

Contrary to the Examiner's contention that "in the instant case the Group II invention could be made by a material different process. For example, selectively forming a first set of dielectric layers into spaced parts to form a first set of openings, instead of forming a first set of dielectric layer to form a first thickness for etching a first set of openings". The Applicants respectfully submit that the present invention structure (claim 18) comprises a first set of dielectric layers that includes a first contact layer comprising a first plurality of metal field openings extending through the first contact layer thickness, and a second set of dielectric layers including a second contact layer overlying the first contact layer comprising a second plurality of metal field openings extending through the second contact layer thickness must be fabricated by a process recited in claim 1, i.e. forming a first set of dielectric layers to form a first thickness for etching a first set of openings through said thickness and forming a second set of dielectric layers to form a second thickness for etching a

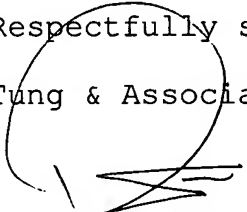
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second set of openings through the second thickness. The method steps proposed by the Examiner of "selectively forming a first set of dielectric layers into spaced parts to form a first set of openings", simply would not work in achieving the present invention structure recited in claim 18.

The restriction requirement imposed by the Examiner is respectfully traversed. A consideration for patentability of Group II, claims 18-37, together with Group I, claims 1-17, is respectfully requested of the Examiner.

Respectfully submitted,

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